REMARKS

The Office Action dated July 12, 2005, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1-10 have been amended. Applicants submit that the new claims as well as the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-10 are pending in the present application and are respectfully submitted for consideration.

Informal Matters

Claim 4 was objected to as containing some minor informalities. In addition, claims 1-10 was rejected under 35 U.S.C. § 112, second paragraph as being indefinite.

Applicant respectfully submits that claims 1-10 have been amended to obviate the claim objection as well as rejection. Accordingly, claims 1-10 are in compliance with US patent practice.

Rejection of Claims 1-3, 5-6 and 8-10 Under 35 U.S.C. § 103(a)

Claims 1-3, 5-6 and 8-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Dhong et al. (US Patent No. 6,014,763, hereinafter "Dhong") in view of Whetsel (US Patent No. 6,405,335). To the extent that the rejection is still applicable, Applicant respectfully traverses the rejection.

Claim 1 recites an integrated circuit comprising, among other features, wherein each of the plurality of boundary scan registers selectively receives and holds one of output data of the corresponding input buffer and the scan-in or scan-out data, and, wherein each of the plurality of boundary scan registers further receives parallel output data of the corresponding serial to parallel conversion circuit and selectively outputs one of the received parallel output data and the held data to an internal circuit.

Claims 5 and 9 each recites an integrated circuit comprising, among other respective features, wherein each of the plurality of boundary scan registers selectively receives and holds one of the output data of the internal circuit, and the scan-in or scan-out data, and wherein each of the plurality of boundary scan registers further receives serial output data of the corresponding output buffer or parallel to serial conversion circuit and selectively outputs one of the received serial output data and the held data to the corresponding output terminal or output buffer.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicant's invention.

Dhong discloses a method of scanning an integrated circuit, by converting a parallel scan input (scan data and scan control) to serial, passing the serial scan input through scan circuitry to create a serial scan output, converting the scan output from serial to parallel, transmitting the scan output in parallel from the integrated circuit to the tester. Dhong further provides a tester clock signal that is derived by synchronizing the tester to a divided clock signal (1/N) of the integrated circuit. Communications take

place at a speed of the tester clock signal, but the scan operates at the full operational speed of the device under test.

Whetsel discloses an integrated circuit comprising core circuitry including functional inputs and functional outputs, an input pad and an output pad. Whetsel also provides a scan distributor circuitry connected between the input pad and, selectively, at least some of the functional inputs, through a multiplexer. Scan collector circuitry connects selectively between at least some of the functional outputs and the output pad, through a demultiplexer. A strobe is inputted to a series of buffers 2208, 2210, 2212, and 2214 connected such that the output of the first buffer drives scan path 1 and the input of the second buffer, the second buffer drives the input of scan path 2 and the input of the third buffer, and so on until the last buffer drives only the last scan path.

Applicant respectfully submits that each of claims 1, 5 and 9 recites subject matter that is neither disclosed nor suggested by the cited prior art. In particular, neither Dhong nor Whetsel, taken together or in combination, disclose or suggest at least the limitations discussed above with respect to each claim. For instance, one embodiment of the present invention provides an integrated circuit having serial to parallel ("S/P") conversion circuits at the input terminals for complying with high speed input signal, in which the signal delay between the input buffer and the S/P conversion circuit becomes smaller. Therefore, the BSR circuits of the present invention can be provided without interfering with a high speed input operation at the input terminal portions.

In contrast, Figure 3 of Dhong merely discloses that the parallel input data from the outside is converted into the serial data for providing to the internal scan path.

Moreover, Dhong only show that the serial data from the internal scan path is converted into the parallel data for outputting to the outside. Also, Figures 3 and 4 of Whetsel merely shows that the serial input data from the outside is converted into the parallel data for providing to the plural internal scan paths, and the parallel data from the plural scan path is converted into the serial data for outputting to the outside.

Applicant submits that in order to establish a *prima facie* case of obviousness, each feature of a rejected claim must be taught or suggested by the applied art of record. See M.P.E.P. §2143.03 and *In re Royka*, 490 F.2d 981 (CCPA 1974). As explained above, Dhong and Whetsel, alone or in combination, do not teach or suggest each feature recited by pending Claims 1, 5 and 9. Accordingly, for the above provided reasons, Applicant respectfully submits that pending Claims 1, 5 and 9 are not rendered obvious under 35 U.S.C. § 103 by Dhong and Whetsel, and therefore, claims 1, 5 and 9 are allowable.

As claims 2-3 depend from claim 1, claims 6 and 8 depend from claim 5, and claim 10 depends from claim 9, Applicant respectfully submit that claims 2-3, 6, 8 and 10 should be deemed allowable for at least the same reasons claims 1, 5 and 9 are allowable, as well as for the additional subject matter recited therein.

Therefore, Applicants respectfully request withdrawal of the rejection.

Rejection of Claims 4 and 7 Under 35 U.S.C. § 103(a)

Claims 4 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Dhong in view of Whetsel and further in view of Lai et al. (US Patent No.

6,763,486, hereafter "Lai"). To the extent that the rejection is still applicable, Applicant respectfully traverses the rejection.

Dhong and Whetsel are discussed above. Lai is relied upon for allegedly teaching that the input and output of an integrated circuit include differential inputs and outputs to the input and output buffers. It is submitted that Lai nevertheless fails to overcome the above-described drawback of Dhong and Whetsel.

As claim 4 depends from claim 1, and claim 7 depends from claim 5, Applicant respectfully submits that claims 4 and 7 should be deemed allowable for at least the same reasons claims 1 and 5, as well as for the additional subject matter recited therein.

Therefore, Applicants respectfully request withdrawal of the rejection.

Conclusion

In view of the above, Applicants respectfully submit that each of claims 1-10 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-10 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **with reference to Attorney Docket number 108066-00037**.

Respectfully submitted,

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Enclosures: Petition for Extension of Time (three months)